

**METHOD AND SYSTEM FOR RECOVERING AND ALIGNING
SYNCHRONOUS DATA OF MULTIPLE PHASE-MISALIGNED
GROUPS OF BITS INTO A SINGLE SYNCHRONOUS WIDE BUS**

ABSTRACT OF THE DISCLOSURE

5 A system for recovering and aligning synchronous data transmissions is disclosed. The system includes a transmitter configured to transmit a source clock signal and a number of data groups over a number of channels with different latencies/propagation delays. The data groups are transmitted during the same clock cycle pursuant to the source clock signal. Each data group is transmitted over a corresponding media channel. The
10 system also includes a receiver configured to receive the source clock signal and the data groups over the corresponding channels and to re-align or recover the wide word that comes in on the channels that are skewed. The receiver further includes: for each channel, (a) a local clock configured to generate a local clock signal based on the source clock signal, the local clock signal being phase-shifted from the source clock signal by a predetermined
15 amount of phase shift, (b) a logic device configured to clock in the data group received over the channel using the local clock signal, (c) a sequence number generator configured to generate a sequence number associated with the data group, (d) a FIFO configured to store and output the clocked-in data group and the associated sequence number, (e) a memory device configured to store the clocked-in data group from the FIFO using the associated
20 sequence number as a memory address, the memory device further configured to output a predetermined portion of its contents after a predetermined capacity threshold is reached. The transmitter is further configured to transmit a start-of-cell signal to the receiver. The sequence number generators are synchronized upon receiving an alignment cell, which is identified by a start-of-cell signal having a specific value for a predetermined cycle period.
25 In one implementation, the receiver is implemented using a number of field programmable gate arrays and the local clocks are implemented using digital clock managers associated with the field programmable gate arrays.